output operation in a processor, the method comprising:

receiving electrical signals representative of an input data vector;

generating electrical signals representative of a condition vector, the number of values in the input data vector being equal to the number of values in the condition vector, values in the input data vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input data vector; and

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generating electrical signals representative of an output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a predetermined value;

wherein generating electrical signals representative of the [plurality of] output [vectors] vector includes:

storing values from the input data vector corresponding to values in the condition vector which are equal to one another in an intermediate memory; and

when the number of values thus stored equals a predetermined number, adding the values to [one of] the output [vectors] vector.

REMARKS

Reconsideration and allowance of the present application are respectfully requested.

Claims 1-18 were presented for examination. Claims 1-6 and 15-18 have been cancelled; thus, claims 7-14 are pending in this application.

The Office Action asserted that the title of the invention was not descriptive. The title of the application has been amended to more specifically describe one aspect of the invention as set forth on page 20 thereof at lines 15-18. Note, however, that this title has merely been revised at the Examiner's request, and changes thereto are in no way intended to act as an estoppel in interpreting the pending claims.

The Office Action requested that the Office Action identify the figure "best representing the invention clearly showing the novelty". Applicants assume this request is for the purpose of identifying the figure to put on the front page of any patent issuing from this application. For that purpose, each of the figures illustrates some aspect of the novelty of a preferred embodiment of the present invention. Applicants prefer that Figure 6, a block diagram conceptually showing how a conditional vector output operation is implemented according to a preferred embodiment of the present invention, be put on the patent's front page. Note, however, that Fig. 6 is in no way intended to represent an estoppel in interpreting the pending claims in the present application.

Claims 3-16 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The claims have been amended to obviate the grounds for this rejection.

Claims 3-6, 15 and 16 have been cancelled, thus rendering the grounds for rejection of those claims moot.

Claim 7 was rejected because the limitations implied by each occurrence of "corresponding to condition vector values" were assertedly ambiguous. In the preferred embodiment, claim 7 generally covers the process of assembling output vectors as described on page 15, line 6 to page 16, line 10 of the present application. Claim 7 has been amended

to more clearly describe features of the present invention.

Applicants submit that the remaining amendments to overcome the § 112 rejection are self-explanatory. In view of the above changes and comments, reconsideration and withdrawal of the rejection under § 112 are respectfully requested.

Claims 1, 2 and 15-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Nguyen. Claims 1, 2 and 15-18 have been canceled, thus rendering the grounds for this rejection moot. In view of the above changes, reconsideration and withdrawal of the rejection under § 102 are respectfully requested.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Koyanagi et al. As noted above, claims 1 and 2 have been cancelled without prejudice. Thus, the grounds for this rejection are moot. In view of the above changes, reconsideration and withdrawal of the rejection under § 102 are respectfully requested.

Claims 15 and 16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Agarwal et al. As noted above, claims 15 and 16 have been cancelled without prejudice. Thus, the grounds for this rejection are moot. In view of the above changes, reconsideration and withdrawal of the rejection under § 102 are respectfully requested.

As noted above, claims 1-6 and 15-18 have been cancelled, leaving claims 7-14. Further, claims 7 and 14 have been rewritten in independent form. Since these claims have not been rejected on prior art grounds, and it is believed that the § 112 rejection of them has been overcome by the above Amendment, it is submitted that these claims are in condition for allowance.

It should be noted that claims 1-6 and 15-18 have been cancelled in this application

merely in order to obtain expedited allowance of the remaining claims which were not rejected on prior art, and not as an acquiescence in the prior art rejections thereof. Applicants plan to file a continuation application to further prosecute these claims.

In view of the above, the subject application is believed to be in condition for allowance and such a Notice is respectfully requested. If anything else is needed to place this application in condition for allowance, the Examiner is respectfully requested to contact the undersigned by telephone.

Respectfully submitted,

PILLSBURY MADISON & SUTRO LLP

By _____

Roger S. Joyner
Reg. No. 36,176
Tel. No.: (650) 233-4552
Fax No.: (650) 233-4545

Pillsbury Madison & Sutro LLP
1100 New York, Avenue, N.W.
Ninth Floor, East Tower
Washington, DC 20005-3918
(202) 861-3000

I certify that this paper is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231, on December 11, 2000

Jeanette Walker

Jeanette Walker-Cooks